

AD-A166 695

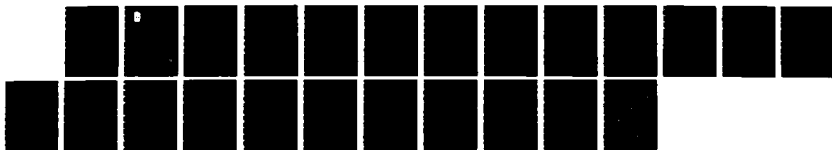
SILICON WAFER CLEANING FOR INTEGRATED CIRCUIT
FABRICATION(U) ROYAL SIGNALS AND RADAR ESTABLISHMENT
MALVERN (ENGLAND) R W HARDEMAN ET AL 1985
RSRE-MEMO-3907 DRIC-BR-98724

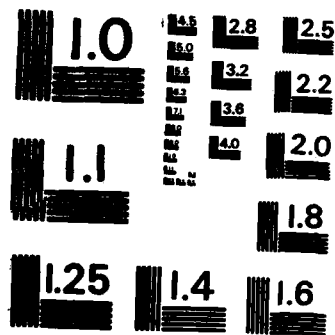
1/1

UNCLASSIFIED

F/G 20/12

NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

UNLIMITED

BR 8724



**RSRE
MEMORANDUM No. 3907**

**ROYAL SIGNALS & RADAR
ESTABLISHMENT**

AD-A166 695

**SILICON WAFER CLEANING FOR INTEGRATED
CIRCUIT FABRICATION**

Authors: R W Hardeman and A M Hodge

RSRE MEMORANDUM No. 3907

DTIC FILE COPY

**PROCUREMENT EXECUTIVE,
MINISTRY OF DEFENCE,
RSRE MALVERN,
WORCS.**

DTIC
ELECTE
APR 15 1986
S D
E

UNLIMITED 86-4 15 223

UNLIMITED

ROYAL SIGNALS AND RADAR ESTABLISHMENT

Memorandum 3907

TITLE: SILICON WAFER CLEANING FOR INTEGRATED CIRCUIT FABRICATION

AUTHORS: R W HARDEMAN* and A M HODGE

DATE: 25th NOVEMBER 1985

SUMMARY

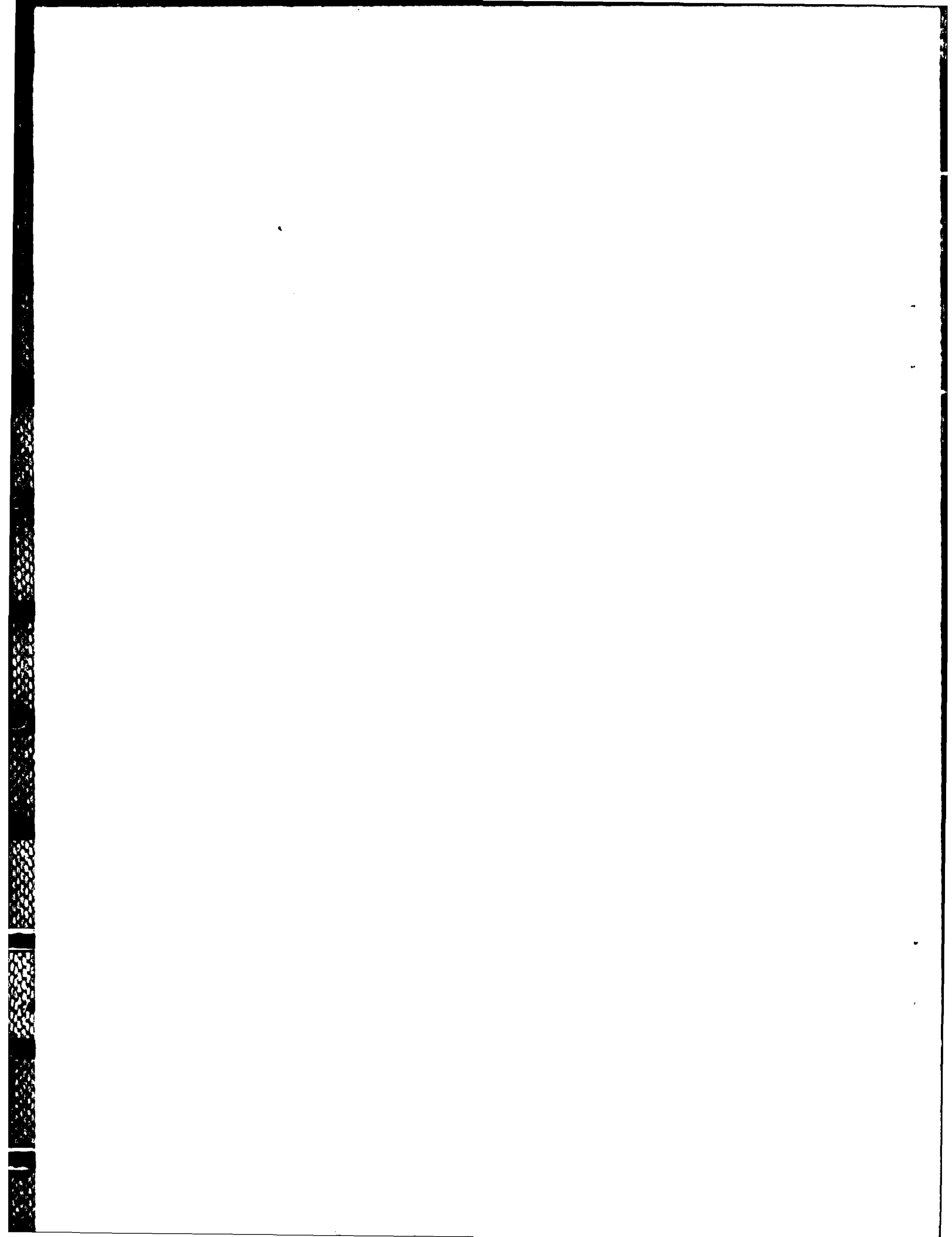
A comparative study has been made of silicon wafers cleaned using different immersion methods in SPEL. The surfaces so produced have been assessed by various methods. The results obtained after using these cleans are reported and shown to be consistent with those described in the literature. The optimum clean has been found to be that described by RCA. This was adopted in SPEL as a standard procedure in August 1984 and results have been encouraging.

* Present address: Data Magnetics, First Avenue, Deeside Industrial Park, Shotton, Clwyd, CH5 2NU, UK

Copyright
C
Controller HMSO London
1985

Accession For	
NTIS GRA&I	<input checked="" type="checkbox"/>
DTIC TAB	<input type="checkbox"/>
Unannounced	<input type="checkbox"/>
Justification	
By	
Distribution/	
Availability Codes	
Dist	Avail and/or Special
A-1	





Contents

Introduction.....	3
Experimental.....	4
Results.....	9
Discussion.....	15
Conclusion.....	18
Acknowledgements.....	18
References.....	19

Introduction

The cleaning of silicon wafers before and during integrated circuit manufacture is of crucial importance to the performance of the devices. The aim of any cleaning process is to remove contaminants and produce a surface free of particulates. Bare silicon is, however, highly reactive so a cleaned surface is, under most conditions, rapidly oxidised and covered by a thin oxide film. In this paper, a 'clean' silicon wafer will be one that has been through an appropriate cleaning schedule and covered by a thin oxide formed in the final stages of that process.

Various recipes for cleaning silicon wafers have been described in the literature [eg 1-5]. The cleaning schedule used in SPEL in SP1 division until August 1984 was based on the RCA clean [1,2]. An alternative was introduced by one of the authors (AMH) for SOS processing in order to reproduce that used at GEC Hirst Research Centre. At about the same time, a high quality cleaning schedule was sought for use on wafers prior to molecular beam epitaxial growth. It became increasingly clear that the relative merits of the different immersion cleans should be investigated and, if possible, a standard, acceptable, characterised and reproducible technique, using the equipment currently available, be adopted for all processing. The purpose of this work was to use the cleaning schedules in SPEL and assess the surface quality so produced, principally for wafers as received from the manufacturers but also for wafers at intermediate stages in the device fabrication sequence. The techniques used for the assessment included ellipsometry (to measure the

thickness and refractive index of oxide layers existing on the wafer surface), laser scattering using commercial equipment (the Surfscan) and X-ray photoelectron spectroscopy (XPS).

Experimental

The wafers used were principally 2" <100> CZ 0.1ohm cm n-type phosphorus doped, supplied by Wacker. Other wafers were, however, used for comparative purposes where appropriate. As received batches were subjected to the cleans listed in Table 1. The chemicals used were Aristar grade supplied by BDH except for the hydrofluoric acid. HF was obtained from Chemwell for reasons which will be discussed below. To simulate cleaning after intermediate device processing steps, certain wafers were cleaned, then oxidised in dry oxygen at 1150°C using a conventional furnace, to produce an oxide 1000Å thick, prior to a second clean and surface analysis.

TABLE 1 CLEANING SCHEDULES

(a) SPEL INITIAL AND PREOX CLEANS -
the cleaning schedules which were in use in SPEL until August 1984

Boil in IPA	10min immersion	\	SPEL initial clean
Rinse in DI	10min		
Boil in H ₂ SO ₄	10min immersion		
Rinse in DI	10min		
Soap solution	10min ultrasonic	\	SPEL preox clean
Rinse in DI	10min		
Bath 1* 35°C	10min immersion		
Rinse in DI	10min		
Bath 2* 35°C	10min immersion		
Rinse in DI	10min		
di:HF 15:1	10s immersion		
Rinse in DI	10min	\	
Spin dry	(includes DI rinse during pre-spin)		

* Bath 1 3:1:1 DI:NH₄OH:H₂O₂* Bath 2 1:1:1 DI:HCl:H₂O₂

All baths at room temperature, (20 - 25°C) except where stated otherwise.

New wafers were treated with the initial and preox clean sequentially but at subsequent stages during processing the preox clean was used alone (whether the clean was prior to oxidation or any other process step).

- (b) BOMB CLEAN -
introduced by AMH for SOS processing
(strictly the H₂SO₄:H₂O₂ mixture is the "bomb")

1:1 H ₂ SO ₄ :H ₂ O ₂	5min immersion	Basic clean
Rinse in DI	10min	
DI:HF 10:1	10s immersion	
Rinse in DI	10min	
1:1 H ₂ SO ₄ :H ₂ O ₂	5min immersion	
Rinse in DI	10min	
DI:HF 10:1	5s immersion	
Rinse in DI	10min	
1% ammonia	10s immersion	
Rinse in DI	10min	
DI:HF 10:1	5s immersion	
Rinse in DI	10min	
1% ammonia	10s immersion	
Rinse in DI	10min	
DI:HF 10:1	5s immersion	
Rinse in DI	10min	
Spin dry	(includes DI rinse during pre-spin)	

All baths at room temperature, except for the H₂SO₄:H₂O₂ mixture, which reached in excess of 100°C on mixing as a result of the exothermic reaction.

The full cleaning schedule listed above was used before gate oxidation but the shorter basic clean was used at other intermediate processing steps.

- (c) RCA CLEAN -
implemented in SPEL following the RCA recipe [3].

Cleaning Procedures for Wafers without or with Thermally-Grown SiO₂ Layers

A. Preliminary Cleaning (if necessary)

1. Remove bulk of photoresist film (if present) by plasma oxidation stripping, or immersion in organic photoresist stripper, or with hot 1:2 vol. to vol. H₂O₂-H₂SO₄ mixture if adequate safety precautions are exercised.
2. Rinse with water (see note on water purity for entire processing).
3. Transfer the wafers to a clean Teflon holder. Pick up wafers only with tweezers of Teflon or polypropylene.

B. Removal of Residual Organic Contaminants and Certain Metals (SC-1)

1. Prepare a fresh mixture of H₂O-NH₄OH-H₂O₂ (5:1:1) by measuring the following reagents into a beaker of fused silica (opaque silica ware is acceptable): a. 5 vol water.
b. 1 vol hydrogen peroxide

(unstabilized electronic grade, w.w%).

- c. 1 vol ammonium hydroxide (electronic grade, 29 w/w% based on NH₃).
2. Stir the solution with a clean rod of fused quartz.
3. Submerge holder with wafers in the cold solution and place the beaker on a hotplate.
4. Heat to 75°-80°C. Then reduce heating to maintain the solution at 80°C for an additional 10 min. (The vigorous bubbling is due to oxygen evolution. Make sure that the solution does not boil so as to prevent rapid decomposition of the H₂O₂ and volatilization of the ammonia).
5. Overflow-quench the solution by placing the beaker under running water for about one minute.
6. Remove holder with wafers and immediately place it in a cascade water rinse tank for 5 min.

C. Stripping of Thin Hydrous Oxide Film from Uncoated Wafers (1:50 HF-H₂O)

1. Submerge wafer assembly from step B-6 directly in an agitated mixture of 1 vol hydrofluoric acid (49%, electronic grade) and 50 vol water. Use a polypropylene beaker for this step.
2. Leave wafers in the solution for only 15 sec. Exposed silicon (but not SiO₂) should repel the HF solution.
3. Transfer wafer assembly to a water tank, but rinse for only 20-30 sec with agitation to remove the HF solution. (This minimizes regrowth of a hydrous oxide film.)
4. Transfer wafer assembly immediately, without drying, into the hot SC-2 solution of step D.

D. Desorption of Remaining Atomic and Ionic Contaminants (SC-2)

1. Prepare a fresh mixture of H₂O-HCl-H₂O₂ (6:1:1) by mea-

suring the following reagents into a beaker of fused quartz:

- a. 6 vol water.
 - b. 1 vol hydrochloric acid (37%, electronic grade).
 - c. 1 vol hydrogen peroxide (30%, unstabilized, electronic grade)
2. Place the beaker on a hotplate and heat to 75°-80°C.
 3. Submerge that still wet wafers in the holder after step B-6 or C-3 in the hot solution.
 4. Maintain the solution at 80°C for 10-15 min.
 5. Overflow-quench as in step B-5.
 6. Continue the rinsing at this stage for a total of 20 min in a cascade rinsing.

E. Drying of the Wafers

1. Transfer the holder with the wet wafers into a wafer centrifuge.
2. Apply a final water rinse during spinning.
3. Allow to dry while gradually increasing the spinning speed (to avoid aerosol formation from the water droplets).

4. Remove the wafers by dump transfer for high-temperature processing. If single-wafer handling must be used, handle the wafers only at the edge with plastic tweezers.

F. Storage

1. Avoid storage of cleaned wafers, preferably by immediate continuation of processing. If storage is unavoidable, store the wafer in closed glass containers cleaned with hot SC-1 solution, followed by water rinsing and oven-drying.

Note concerning processing water and reagents — All water used for preparing the reagent mixtures or for rinsing should be thoroughly deionized and ultrafiltered, with a resistivity in the 10-20 megohm range at 18°-23°C. All reagents should be electronic grade, preferably ultrafiltered for freedom from particulate impurities. Operations should be conducted in a clean room environment to avoid recontamination.

The thickness of the oxide on the wafers as supplied by the manufacturers, and at various stages through the cleaning process was measured using the Nanospec (Nanometrics Inc.) or by single wavelength (He Ne 632.8nm) ellipsometry. Psi and delta values were converted to thickness and refractive index using the programme due to McCrackin et al [6].

The Surfscan (Tencor Inc.) was used to check the particulate contamination on the silicon surfaces at various stages in processing.

XPS was carried out in the preparation chamber of a diffusion-pumped, load-locked Si-MBE system (VG366) operated at $<1\text{E}-8\text{mbar}$. It is, therefore, important to point out that all samples so examined will have undergone pump-down from atmospheric pressure to UHV, over a period of about one hour. Under these conditions it is possible that volatile components have been lost from the sample surfaces.

XPS was used deliberately for two reasons. First it is an averaging technique, over some $5\text{mm} \times 5\text{mm}$ of the wafer surface and secondly to avoid electron-beam stimulated effects (oxide desorption, carbon contamination) which may arise during extended use of the alternative Auger electron spectroscopy to examine thin silicon oxides. Calibration of the electron spectrometer and the monitoring of surface charging were carried out using standard techniques [7]. Survey spectra over 1250eV scans were employed, supplemented by high-resolution (100meV) spectra (Si 2p, C 1s, O 1s) collected at 40meV/s scan rates.

The Si 2p spectra have been shown [8] to contain information on the oxidation state and bonding character of the Si atoms which are probed ie within the escape depth of electrons in the Si/SiO₂ system. The areal or height ratio of the subpeaks in these spectra can give an indication of the relative proportions of atoms present in various oxidation states, and hence when suitably calibrated, a measurement of the oxide thickness. This technique has high sensitivity in the range of oxide thickness (10 - 60Å), of specific interest in this study.

The overall sensitivity of XPS is on the order of 1% of a monolayer of uniformly distributed contaminant. It is not therefore adequate to investigate trace metal contamination. This study, using static and dynamic Secondary Ion Mass Spectrometry (SIMS), is continuing on silicon/silicon oxide interfaces and on the substrate/epilayer interface of MBE grown Si epilayers prepared on cleaned wafers. The electrical properties of oxides grown on cleaned wafers were assessed by using them as the dielectric in conventional MOS capacitor structures.

Results

Wafers as received from the manufacturers are covered by a thin oxide which grows during and after wafer cleaning following polishing. The thickness of this film is difficult to measure absolutely without resorting to spectroscopic ellipsometry. The thicknesses measured in this study agreed

with the accepted value of approximately 15\AA . Silicon wafers are hydrophilic because of this native oxide coating them, but 15s etch in HF (1:50 HF in water) is sufficient to remove this leaving bare silicon which is hydrophobic. In normal atmospheric conditions, a bare silicon surface reacts rapidly and a thin oxide film about 15\AA thick reforms.

Visually, the different cleaning procedures did not show any distinguishing features except for the IPA boil at the beginning of the SPEL initial clean. On removing the wafers from the warm solution it evaporated quickly to leave a streaky, milky film across the surfaces. The formation of deposits following solvent cleans of various materials is known (eg on LiNbO_3 slices used for surface acoustic wave device fabrication, [9]).

The oxide removal during an RCA clean has been measured on the silicon wafers which had 1000\AA oxide grown thermally on the surface. The oxide thickness was measured on the Nanospec after bath 1, the HF dip and bath 2. The averaged results are presented in Table 2.

TABLE 2. OXIDE THICKNESS AT STAGES THROUGH RCA CLEANING

Oxidised wafer		1047 \AA
Bath 1		1043 \AA
HF dip		1018 \AA
Bath 2		1018 \AA

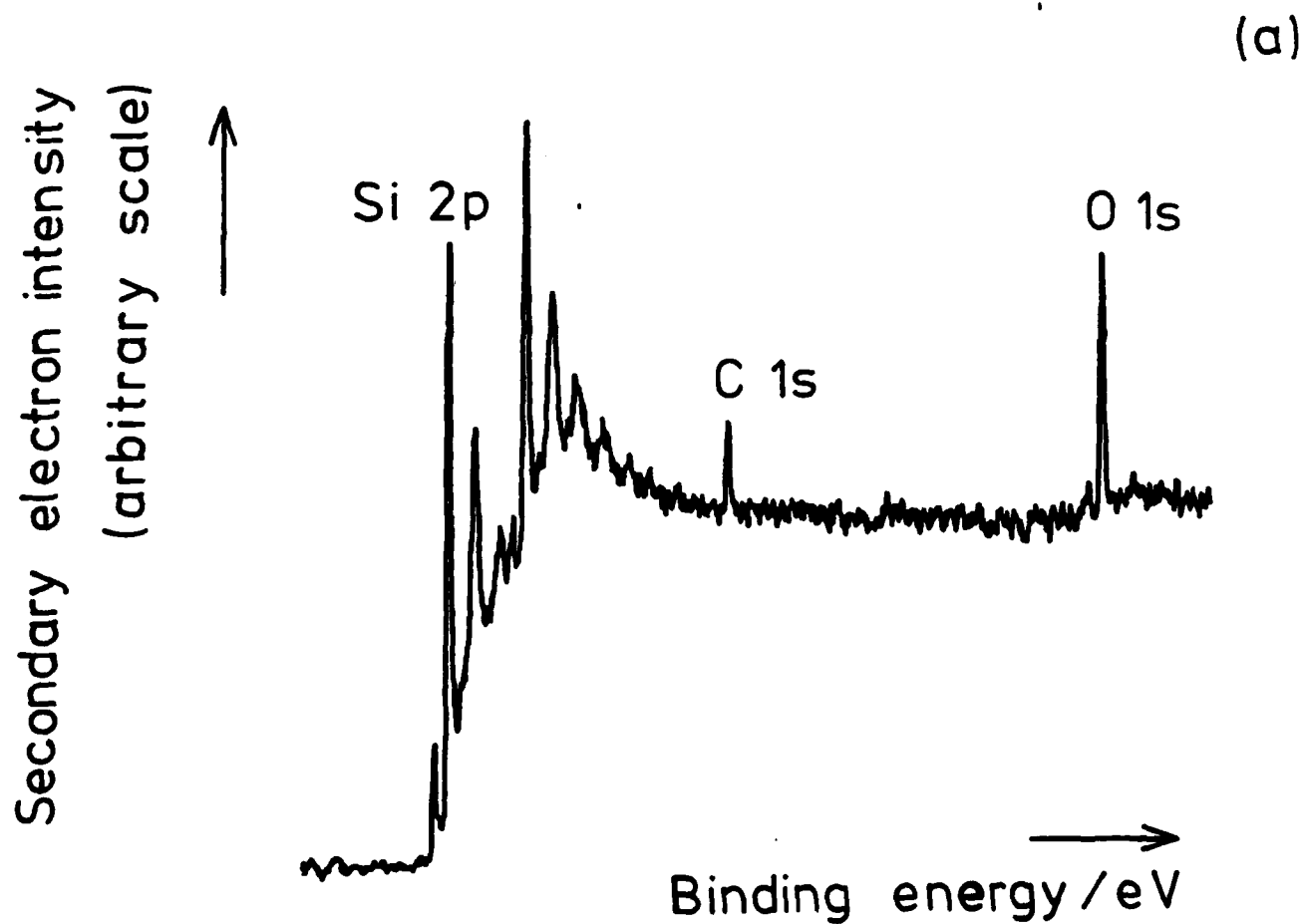
Total oxide removal		29 \AA

The oxide removal during a clean is obviously not important for thick oxides (eg field oxides typically $1\mu\text{m}$ thick). However, for thin (gate)

oxides, generally $<1000\text{\AA}$, the thickness removed is more significant. With the trend to thinner gate oxide layers 300\AA , the amount etched off becomes proportionately more important, particularly when several cleans are carried out with the same oxide exposed.

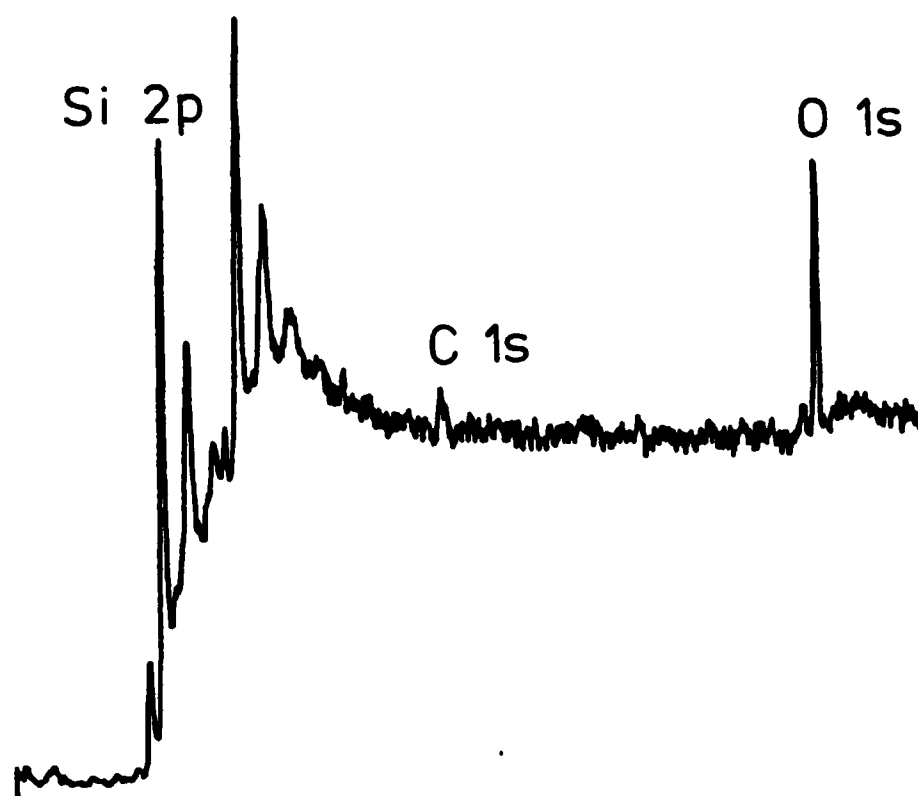
Representative XPS survey spectra taken on freshly prepared cleaned wafers are shown in figure 1 in which the principal peaks of interest have been identified. As was expected, the SPEL clean finishing with the HF etch, showed the least oxide. It also showed the greatest carbon. The RCA clean resulted in the highest oxide peak and modest carbon. In terms of carbon removal alone, the bomb clean was slightly better but no sulphur was detected as has been reported previously after use of these reagents [5].

Figure 1 Representative XPS survey spectra after various cleaning schedules
(a) SPEL clean, (b) 'Bomb' clean, (c) RCA clean.

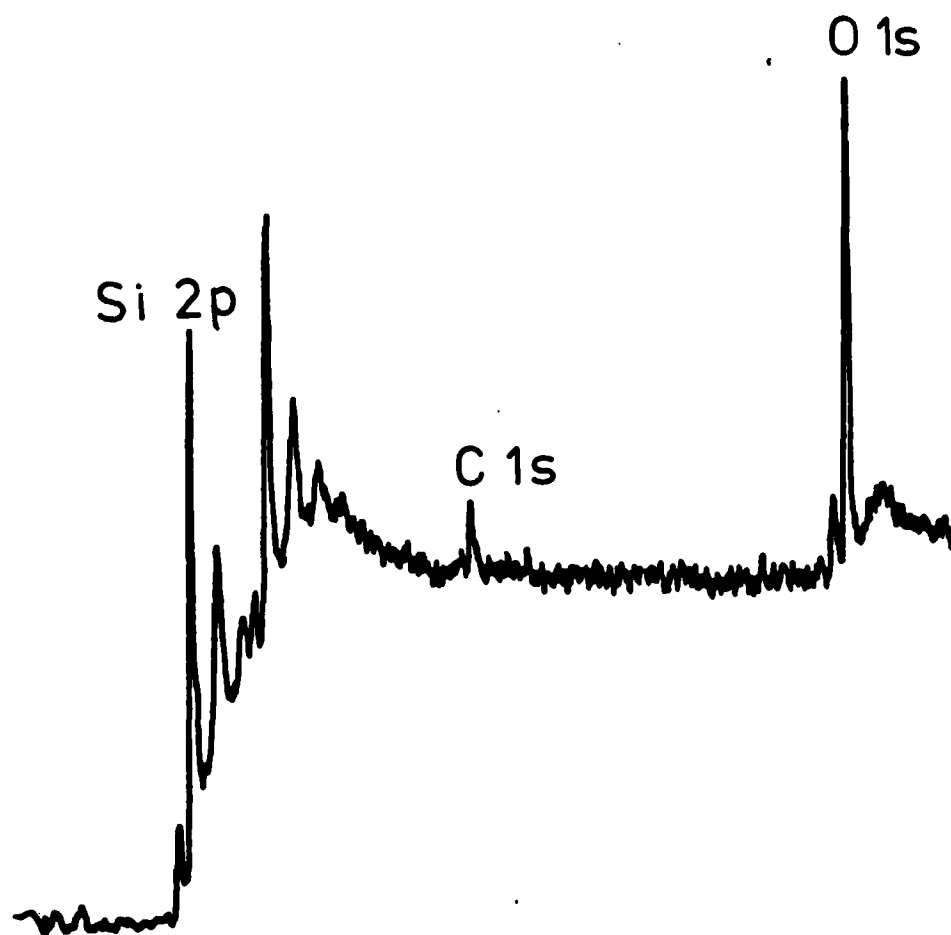


(b)

13



(c)



The Surfscan (see [10] for details of the information obtainable with this instrument) shows that as received wafers are virtually free of particulates (<10 defective cells) larger than $1\mu\text{m}$ - the minimum size detectable with the instrument in use. After cleaning, the particulate count is increased (on average 400 defective cells per 2" wafer). This is concerning but not entirely unexpected as the chemicals in use in SPEL are neither semiconductor grade nor assessed for particulate levels. In particular, it was found prior to this study that BDH acid was badly affected by particulate contamination and that this, in turn seemed to be responsible for excessive defective cell counts recorded with the Surfscan on cleaned wafers. It was for this reason that HF was obtained from Chemwell after nominal filtration to $0.2\mu\text{m}$.

The haze value measured by the Surfscan is very constant (between 50 and 100) for both as received and cleaned wafers. After furnace oxidation the haze value falls to values less than 30; this is probably due to the change in submicron scale surface texture from a bare silicon surface (albeit with a thin native oxide) to a thicker oxide film.

The main practical disadvantage of the RCA or SPEL clean is the time taken to heat sufficient solution in bath 1 and bath 2 to the recommended temperature to submerge a cassette of 3" wafers. For the bomb clean, the heat of reaction on adding the acid to the peroxide heats the solution to a suitable temperature but the bath temperature is not controlled.

Wafers cleaned using the RCA recipe have been used in this study as substrates for MBE growth. The oxide produced by this clean is clearly less stable towards thermal desorption in UHV than is the oxide on as received wafers. Transient Mass Spectrometry has been used to monitor the desorption process [11] and the properties of the grown epilayers and nature of the interfaces produced is the subject of further study. The RCA cleaned wafers have also been used routinely in device fabrication with no adverse results. Standard gate oxides grown on the RCA cleaned wafers and incorporated in conventional metal gate MOS capacitors showed acceptable electrical characteristics with the density of interfaces at mid band gap better than $1\text{E}11\text{ cm}^{-2}\text{eV}^{-1}$.

Discussion

The cleaning schedules used in these experiments all aim to produce a 'clean' silicon surface as defined in the Introduction above. It is therefore useful to compare the relative merits of the three cleans used in this study. The sulphuric acid / hydrogen peroxide clean (variously called 'bomb', Piranha [4] or Caro's acid [5]) is reputedly almost as effective as the RCA recipe for the removal of organics and metallics but the products are not as volatile. In this study it has been found to be the most efficient at removing carbon from the wafer surface. Although none was evident in this study, there is also a risk of sulphur deposition from the sulphuric acid [5] and the mixture is quoted as being potentially hazardous.

The RCA bath 1 (ammonia / hydrogen peroxide solution with high pH) aims to remove any organic material first by the solvating action of the ammonia and oxidising action of the peroxide with the formation of volatile products. It can also complex some group I and II metals. Bath 2 (hydrochloric acid / hydrogen peroxide solution with low pH) removes inorganics by complexing and production of volatile species. Further work from RCA proposed the addition of an HF etch between bath 1 and bath 2 in order to remove the native oxide immediately prior to bath 2 so that the inorganic contaminants on the silicon itself are removed as efficiently as possible [2]. Recently the merits of this sequence has been justified [3].

The SPEL preox clean used the same solutions as that described by RCA but with different proportions in the mixtures, in a different order and without the optimised times, temperatures etc. now advocated in the literature [3]. In addition, several extra stages (the initial clean) were used before baths 1 and 2 and HF dip. In this study we found that a boil in IPA tended to produce a deposit on the wafer surface which was subsequently very difficult to remove although the principal objective of this stage was to remove organic contamination. Also the carbon contamination level was greatest after this cleaning schedule confirming a previous report [13]. This is of particular concern for the preparation of wafers for MBE or CVD growth. The requirements for MBE growth in particular have been described in the literature [12]. A thin oxide, carbon-free at its interface with the substrate Si and through its thickness, which is desorbed on heating in UHV and/or exposure to a flux of Si is the essential aim.

The position of the HF dip also warrants discussion. In the SPEL clean this was carried out as the final step before the rinse and spin dry. This poses several potential problems: (i) For new silicon wafers this HF etch removes entirely the native oxide present leaving a highly reactive, bare silicon surface. This re-oxidises rapidly under whatever laboratory ambient prevails subsequently. If the HF etch is before bath 2, the oxide film reforms in controlled conditions in the solution. (ii) HF is difficult to obtain with very high purity and there is consequently a risk of residual contamination from this reagent if used in the final cleaning step. HF has also been suspected of leaving contamination during anodisation to form porous silicon [14,15]). In comparison, if the HF etch is carried out before bath 2, as initially proposed by RCA [2], the bare silicon surface so created is exposed to the reagents of bath 2 so metallic contaminants in the silicon itself should be removed more efficiently than if an oxide film were present. Also, if the HF were to leave any impurities they should, in turn, be removed by the action of bath 2 when it follows.

As a result of these studies the RCA clean was adopted as a standard in SPEL following the prescribed recipe as closely as possible [3]. Although the bomb clean resulted in slightly lower carbon levels, it was felt that the uncontrolled solution temperatures [16], reported sulphur and heavy metal contamination (not assessed in this study) were factors against its adoption. The RCA clean is used for new wafers received from the manufacturers and also at intermediate stages during processing. The fact that approximately 30Å oxide is removed by this treatment must, however be considered particularly

where critical, thin gate oxides are exposed to the reagents. Since the adoption of the RCA clean consistent results have been obtained.

In this study immersion cleans have been used exclusively - no attempt has been made to assess some of the alternative spray or non-contact brush systems. It is possible, particularly with regard to the particulate levels, that one of these mechanical cleans may be required in addition in the future [17].

Conclusion

Silicon wafers have been cleaned using various recipes described and the surface quality assessed principally by XPS. As a result of these studies it was decided to use the RCA clean [3] in SPEL as standard for new and partly processed wafers. This was adopted in August 1984 and to date the reproducibility has been good.

Acknowledgements

Acknowledgement is due to C Pickering for the ellipsometry analyses and to T Janes, P C Stevens, M Roberts and P Henton for particulate contamination investigations prior to this study.

References

1. W Kern and D A Puotinen, RCA Review, p187, June 1970
2. J A Amick, Solid State Technology, p47, November 1976
3. W Kern, Semiconductor International, p94, April 1984
4. B F Phillips, D C Burkman, W R Schmidt and C A Peterson, J. Vac. Sci. Tec., A1 (2), p646, Apr-Jun 1983
5. D Burkman, Semiconductor International, p103, July 1981
6. F L McCrackin, E Passaglia, R R Stromberg and H L Steinberg, J. Res. NBS 67A, 4, p363, 1963
7. C D Wagner, ASTM STP 699, 1980
8. E Mello Ceresa and F Garbassi, Materials Chemistry and Physics, 9, p371, 1983
9. A M Hodge, RSRE Memo No. 3502, 1982
10. Surfscan Operators Manual, revised edition
11. R W Hardeman, D J Robbins, D B Gasson and A Daw, Proc. Electrochem. Soc. 1st MBE Symposium, Toronto 1985
12. J C Bean, Chap. 4 in Materials Processing Theory and Practices, Vol. 2, Impurity Doping Processes in Silicon, Ed. F F Y Wang, North-Holland, 1981
13. R C Henderson, J. Electro. Chem. Soc., 119, p772 June 1972
14. R C Frye, Mat. Res. Soc. Symp., 33, p53, 1984
15. M I J Beale, Unpublished results
16. F Pitchovski, J. Electro. Chem. Soc., 126, p1428, August 1979
17. P S Burggraaf, Semiconductor International, p71, July 1981

DOCUMENT CONTROL SHEET

Overall security classification of sheet UNCLASSIFIED *AD-A166695*

(As far as possible this sheet should contain only unclassified information. If it is necessary to enter classified information, the box concerned must be marked to indicate the classification eg (R) (C) or (S))

1. DRIC Reference (if known)	2. Originator's Reference MEMORANDUM 3907	3. Agency Reference	4. Report Security U/C Classification	
5. Originator's Code (if known)	6. Originator (Corporate Author) Name and Location ROYAL SIGNALS AND RADAR ESTABLISHMENT			
5a. Sponsoring Agency's Code (if known)	6a. Sponsoring Agency (Contract Authority) Name and Location			
7. Title SILICON WAFER CLEANING FOR INTEGRATED CIRCUIT FABRICATION				
7a. Title in Foreign Language (in the case of translations)				
7b. Presented at (for conference papers) Title, place and date of conference				
8. Author 1 Surname, initials HARDEMAN, R W	9(a) Author 2 HODGE, A.M.	9(b) Authors 3,4...	10. Date	pp. ref.
11. Contract Number	12. Period	13. Project	14. Other Reference	
15. Distribution statement HEAD SP GROUP				
Descriptors (or keywords)				
continue on separate piece of paper				
Abstract A comparative study has been made of silicon wafers cleaned using different immersion methods in SPEL. The surfaces so produced have been assessed by various methods. The results obtained after using these cleans are reported and shown to be consistent with those described in the literature. The optimum clean has been found to be that described by RCA. This was adopted in SPEL as a standard procedure in August 1984 and results have been encouraging.				

END

Dtic

5-86